REMARKS

Claims 27 and 32-35 are pending in this application. Claims 27 and 32-35 have been amended. No new matter has been introduced.

The drawings stand objected to as "they do not include the following reference sign(s) mentioned in the description (see, e.g., par. 0041/ll.6) with respect to figure 19: 100." (Office Action at 2). Applicants submit that NMOS transistor 100 is illustrated in Figure 20. Applicant also submits that paragraph [0070] of the specification has been amended to clarify that NMOS transistor 100 is illustrated in Figure 20 and not in Figure 19.

Claims 27, 32 and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu (U.S. Patent No. 6,484,065) in view of Houston (U.S. Patent No. 6,424,016) and King (U.S. Patent No. 6,754,104). This rejection is respectfully traversed.

Amended independent claim 27 recites a "processor system" comprising "a processor" and "an integrated circuit coupled to said processor, at least one of said integrated circuit and processor comprising a fully-depleted SOI NMOS transistor as part of a memory array, said fully-depleted SOI NMOS transistor comprising first source and drain regions provided on a SOI substrate, said first source and drain regions being of n-type conductivity" and "a first gate stack fabricated on said SOI substrate, said first gate stack including a doped silicon/germanium layer of p-type conductivity." Amended independent claim 27 also recites "a partially-depleted SOI NMOS transistor as part of a periphery array, said partially-depleted SOI NMOS transistor comprising second source and drain regions provided on said SOI substrate, said second source and drain regions being of n-type conductivity" and "a second gate

stack fabricated on said SOI substrate, said second gate stack including a conductive layer of n-type conductivity."

Yu relates to "digital signal processing (DSP)." Yu teaches that "efficient DSP or MPU is combined with efficient DRAM on a single IC die." (Abstract). According to Yu, "[t]o optimize the embedded memory, the chip includes wide-band connections to DRAM" so that "[r]ow and column addresses of DRAM can be applied at the same time using wide address busses." (Abstract).

Houston relates to a DRAM having a SOI substrate with the same conductivity type transistors in the periphery and array area. According to Houston, the DRAM includes "a memory array including a plurality of pass gate transistors and a plurality of memory elements." (Abstract). Houston also teaches that "[t]he pass gate transistors include a gate material selected to provide a substantially near mid-gap work function or greater." (Abstract).

King relates to a "semiconductor device including integrated insulated-gate field-effect transistor (IGFET) elements and one or more negative differential resistance (NDR) field-effect transistor elements, combined and formed on a common substrate." (Abstract). King teaches that "[B]ecause both types of elements share a number of common features, they can be fabricated with common processing operations to achieve better integration in a manufacturing facility." (Abstract).

The subject matter of claims 27, 32 and 33 would not have been obvious over Yu, Houston and King, whether considered alone or in combination. Specifically, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or

in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

First, Yu, Houston and King, whether considered alone or in combination, fail to disclose, teach or suggest all limitations of claim 27. Yu is silent about "at least one of said integrated circuit and processor" comprising "a fully-depleted SOI NMOS transistor as part of a memory array" and "a partially-depleted SOI NMOS transistor as part of a periphery array," as independent claim 27 recites. Yu does not even mention a "SOI substrate," much less a "SOI substrate" on which fully-depleted and partially-depleted transistors having the specific characteristics recited in claim 27 are formed in the memory and array areas, respectively.

Houston also does not disclose, teach or suggest "a processor," much less "an integrated circuit coupled to said processor," wherein at least one of said integrated circuit and processor comprises SOI NMOS transistors, as in the claimed invention. Houston is also silent about "a fully-depleted SOI NMOS transistor as part of a memory array . . . comprising first source and drain regions . . . of n-type conductivity; and a first gate stack . . . including a doped silicon/germanium layer of p-type conductivity" and "a partially-depleted SOI NMOS transistor as part of a periphery array . . . comprising second source and drain regions . . . of n-type conductivity; and a second gate stack . . . including a conductive layer of n-type conductivity," as in the claimed invention. Houston teaches only that p+polysilicon gate material is employed for "(1) Pass transistors: fully depleted p-channel transistors having n-doped poly gates with

1E17 n type doping in channel. (Vt=.about.-1.2V)" and "(3) p-channel periphery transistors: partially depleted transistors having p-doped poly gates with 6E17 n type doping in channel. (Vt=.about.-0.5V)." (Col. 6, lines 15-24). Thus, Houston is silent about the characteristics of the fully-depleted and partially-depleted SOI NMOS transistors of the claimed invention.

Houston also does not disclose, teach or suggest "a first gate stack . . . including a doped silicon/germanium layer of p-type conductivity" as part of a "fully-depleted SOI NMOS transistor . . . of a memory array," much less "a first gate stack . . . including a doped silicon/germanium layer of p-type conductivity" as part of a "fully-depleted SOI NMOS transistor . . . of a memory array" and further as part of a "processor-based system" comprising "a processor" and "an integrated circuit coupled to said processor," as in the claimed invention

King does not rectify the deficiencies of Yu and Houston. King does not disclose any of the limitations of claim 27. King teaches integration of "one or more negative differential resistance (NDR) field-effect transistor elements" with field effect transistors on a common substrate, and not the limitations of the claimed invention.

Second, to establish a *prima facie* case of obviousness, "[i]t is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor." Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934 (Fed. Cir. 1990). This way, "the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." Hartness Int'l, Inc. v. Simplimatic Engineering Co., 819 F.2d 1100, 1108 (Fed. Cir. 1987). Accordingly, a determination of obviousness "must involve more than indiscriminately combining prior art; a motivation or

suggestion to combine must exist." Pro-Mold & Tool Co., 75 F.3d at 1573. This way, a rejection of a claim for obviousness in view of a combination of prior art references must be based on a showing of a suggestion, teaching, or motivation that has to be "clear and particular." In re Dembiczak, 175 F.3d at 999. Thus, the mere fact that it is possible to find three isolated disclosures which might be combined to produce a new structure does not necessarily render such process obvious, unless the prior art also suggests the desirability of the proposed combination.

The May 23, 2006 Office Action fails to establish a *prima facie* case of obviousness because, as the Court in Northern Telecom, Inc. noted, "[i]t is insufficient that the prior art disclosed the components of the patented device" and there is no "teaching, suggestion, or incentive to make the combination." Northern Telecom, Inc., 908 F.2d at 934. On one hand, the crux of Yu is optimizing an embedded memory by providing the chip with wide-band connections to DRAM, so that "[r]ow and column addresses of DRAM can be applied at the same time using wide address busses." (Abstract). On the other hand, the crux of Houston is a DRAM having a SOI substrate with the same conductivity type transistors in the periphery and array area. For this, Houston teaches that pass gate transistors are selected to "include a gate material selected to provide a substantially near mid-gap work function or greater." (Abstract). The crux of King is the integration of "one or more negative differential resistance (NDR) field-effect transistor elements" with field effect transistors on a semiconductor substrate. Accordingly, a person of ordinary skill in the art would not have been motivated to combine these three disparate references, and withdrawal of the rejection of claims 27, 32 and 33 is respectfully requested.

Claims 34 and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu/Houston/King in view of Wu (U.S. Patent No. 6,060,749). This

rejection is respectfully traversed.

Claims 34 and 35 depend on independent claim 27 and recite that "at least one of said first and second gate stacks further comprises a silicide layer over said conductive layer" (claim 34) and that "at least one of said first and second gate stacks further comprises a cap layer over said conductive layer" (claim 35).

Wu relates to a "SOI structure formed in a substrate" having a gate "formed over the substrate in a recessed portion of a substrate." (Abstract). According to Wu, "[A] first isolation structure is formed on the side walls of the gate" and "[A] second isolation structure is formed adjacent to the first isolation structure." (Abstract). Wu also teaches that a first metal silicide layer "is formed on the source and drain regions and a second metal silicide layer is formed on the gate." (Abstract).

The subject matter of claims 34 and 35 would not have been obvious over Yu, Houston, King and Wu, considered alone or in combination. As noted above, Yu, Houston and King, alone or in combination, do not disclose or suggest all limitations of independent claim 27. Wu does not rectify the deficiencies of Yu, Houston and King. Wu teaches the formation of a gate structure in a recessed portion of a substrate, wherein a field oxide FOX region 14 is first formed, followed by the formation of an opening 12 in the FOX region 14, and the formation of oxynitride layer 22 and gate layer 24 in the opening. Wu also teaches that remaining FOX region 14 is removed to allow spacers 32 to be formed on the sides of the gate layer 24. Thus, Wu teaches a very specific method for the formation of a gate stack in a recessed region of a substrate, and none of the limitations of independent claim 27. For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness and withdrawal of the rejection of claims 34 and 35 is respectfully requested.

Allowance of all pending claims is solicited.

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Respectfully submitted,

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